

Introduction

This short document describes the circuit for a Xilinx Parallel/JTAG Download Cable. This document is provided free of charge, with no warranty, to support anybody who wishes to construct one of these cables.

The cable connects to the parallel port on a PC and allows the Xilinx FPGA on the E7T-DBoard to be configured directly using the IMPACT program that is part of Xilinx's ISE software suite.

The cable described in this document is based on a schematic diagram from Xilinx's website:
http://toolbox.xilinx.com/docsan/2_1i/data/common/hug/fig13.htm

This cable is also compatible with the open source software package 'Jtag Tools' (see: <http://openwincc.sourceforge.net/jtag/>). Using this package with the download cable allows a PC to connect to and control any JTAG hardware, not just Xilinx FPGAs.

Notes:

This document contains a schematic diagram, a Bill Of Materials and a stripboard layout for the circuit. This stripboard layout has been used to make many of these cables at Sweeney Design without any problems.

The cable between the DB25 male connector and the circuit board should be from 1½ to 2 meters long, and needs to be multi-core cable. For this we generally use 8-core signal/burglar alarm cable.

The JTAG connector and fly leads that connects the download cable to the JTAG connector on the target board is available from Xilinx (Part Number: HW-FLYLEADS) for \$15 (USD):

(http://www.xilinx.com/xlnx/xebiz/productview.jsp?BV_SessionID=@@@1481260731.1070793360@@@&BV_EngineID=ccccadcjmhjdgceflgcefldfgldgji.0&sGlobalNavPick=&sSecondaryNavPick=&category=-19314&iLanguageID=1). This connector simply plugs onto the 9x1 way pin strip connector (J2) on the stripboard and provides fly leads to connect to the target board.

The 9x1 way pin strip connector (J2) should have its unused pins (3, 5, and 8) snipped off with wire cutters.

The box to house the circuit board can be any suitably sized box.

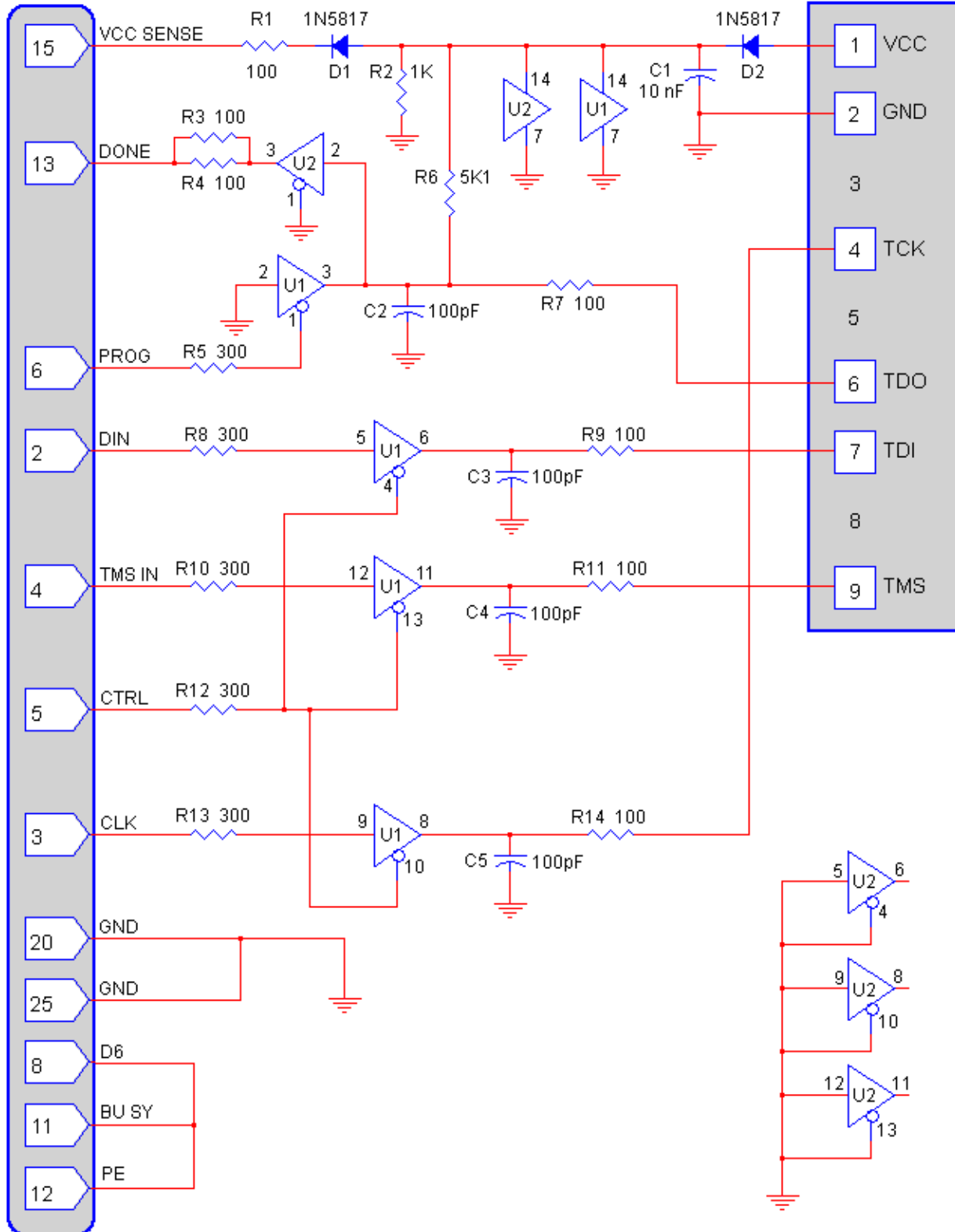
Bill Of Materials (BOM)

| Part Type | Package | Qty | Ref Designator | Description |
|-----------------------|-------------|-----|------------------------------|--|
| Semiconductors | | | | |
| 74HC125 | 14 pin DIL | 2 | U1, U2 | Quad bus buffer |
| 1N5817 | DO41 | 2 | D1, D2 | Schottky rectifier diode |
| Resistors | | | | |
| 100R | Leaded | 7 | R1, R3, R4, R7, R9, R11, R14 | Resistor (5%, 1/8W) |
| 1K | Leaded | 1 | R2 | Resistor (5%, 1/8W) |
| 300R | Leaded | 5 | R5, R8, R10, R12, R13 | Resistor (5%, 1/8W) |
| 5K1 | Leaded | 1 | R6 | |
| Capacitors | | | | |
| 10nF | 0.1" Leaded | 1 | C1 | Ceramic Capacitor (100V) |
| 100pF | 0.1" Leaded | 4 | C2, C3, C4, C5 | Ceramic Capacitor (100V) |
| Connectors | | | | |
| DB25 (Male) | | 1 | J1 | DB25 Male Connector |
| 9x1 way Pin Strip | 0.1" Pitch | 1 | J2 | Pin Strip to accept JTAG fly leads |
| Misc | | | | |
| JTAG fly leads | | 1 | N/A | Parallel Cable Fly leads (from Xilinx) |
| Box | | 1 | N/A | Box to house circuit board |

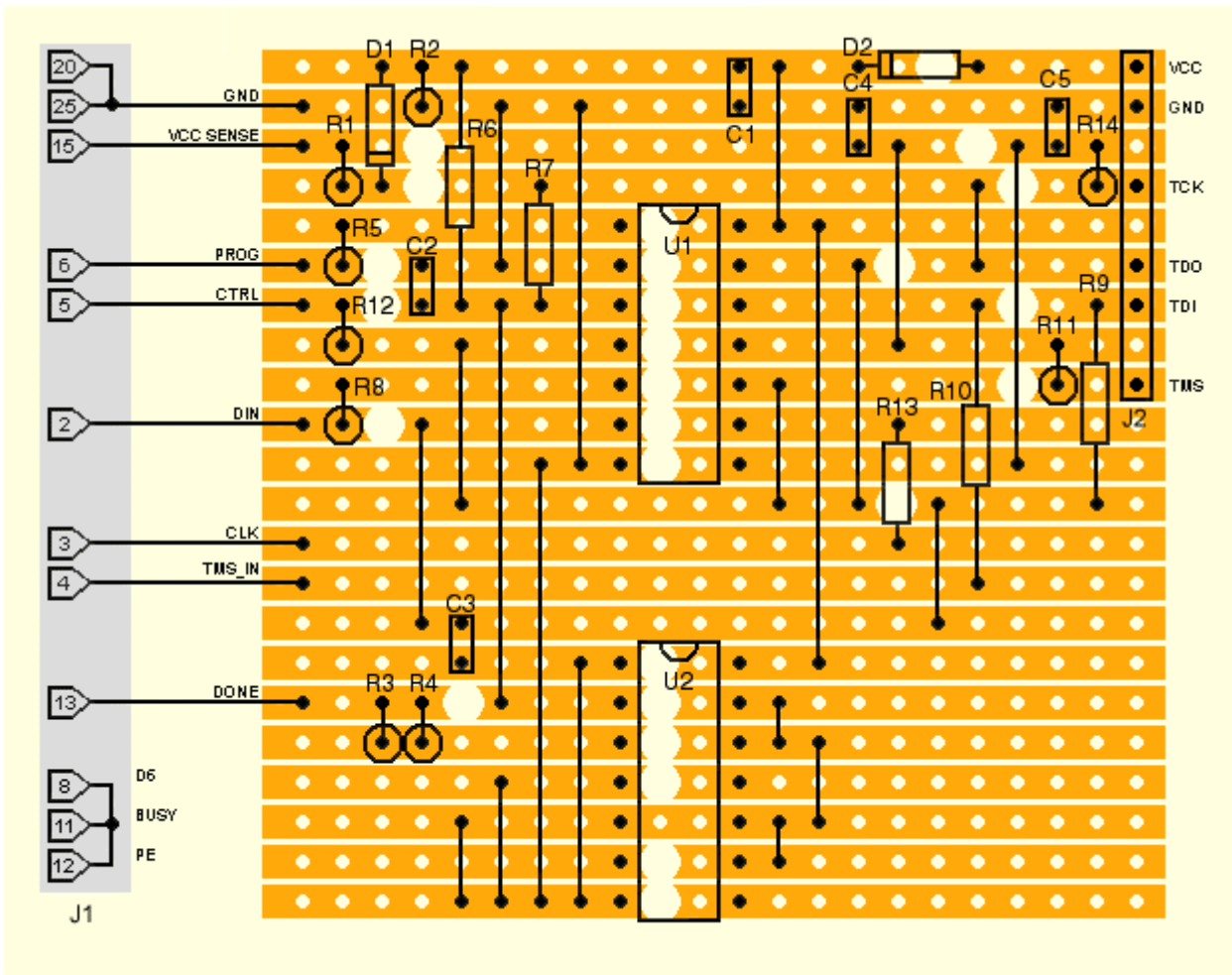
Schematic Diagram

DB25 MALE
CONNECTOR

JTAG Header



Stripboard Layout



Note: pins 8, 11 and 12 of the DB25 male connector (J1) are connected together inside the connector housing. This is also true for pins 20 and 25.