

General Description

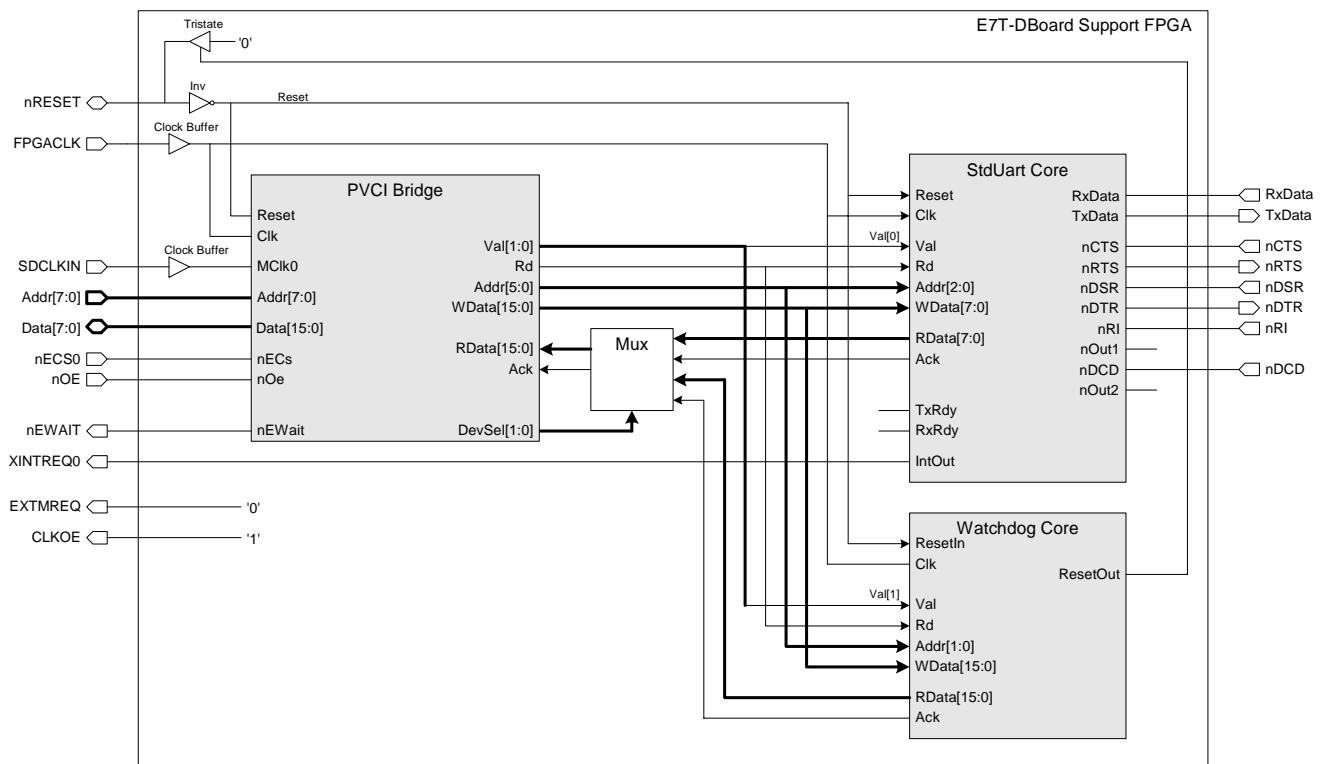
The E7T-DBoard Support FPGA Image is a pre-built FPGA image containing a StdUart core, a Watchdog core and a KS32C50100 processor to PPCI bridge core. This FPGA image is supplied to allow software engineers that are not using the FPGA for development to utilise the FPGA. This FPGA image adds an extra UART and a watchdog timer to the E7T-DBoard.

FPGA Image Files

The StdUart FPGA Image consists of 1 file:

supportfpga.bit – Bit file for Xilinx XC2S200-6 FPGA.

Block Diagram



FPGA Configuration

The StdUart FPGA Image was configured to use a JTAG clock as the FPGA startup clock. Therefore this image can be used to configure the FPGA using either a Xilinx download cable connected to the E7T-DBoard JTAG connector or using the RedBoot firmware with the additional fpgaload command included. See the E7T-DBoard Reference Manual for more details.

The StdUart FPGA Image is not suitable for writing to a Xilinx EEPROM to configure the FPGA, this requires an image configured to use a CCLK as the FPGA startup clock.

PvciBridge Core Generics

The PvciBridge core generics were set to the values in the table below for synthesis:

Generic	Value	Description
gAddrInWidth	8	Width of input address bus.
gAddrOutWidth	6	Width of output address bus.
gDataWidth	16	Width of input and output data bus.
gNumOfDevs	2	Number of PVC I devices.

StdUart Core Generics

The StdUart core generics were all set to their default values for synthesis. These values are listed in the table below:

Generic	Value	Description
gTxFifoDepth	16	Transmit FIFO depth.
gRxFifoDepth	16	Receive FIFO depth.
gFifoTrig0	1	Receive FIFO interrupt trigger level when FCR[7:6] = 00.
gFifoTrig1	4	Receive FIFO interrupt trigger level when FCR[7:6] = 01.
gFifoTrig2	8	Receive FIFO interrupt trigger level when FCR[7:6] = 10.
gFifoTrig3	14	Receive FIFO interrupt trigger level when FCR[7:6] = 11.
gExtndRd	0	0 = Normal read accesses. 1 = Extended read accesses.

Watchdog Core Generics

The Watchdog core generics were all set to their default values for synthesis. These values are listed in the table below:

Generic	Value	Description
gExtndRd	0	0 = Normal read accesses. 1 = Extended read accesses.
gClkDivisor	39999	Amount (less 1) to divide the main clock to produce the prescale clock.

FPGA Pinout

Signal Name	FPGA Pin #	Pin Type	Description
System Ports			
nRESET	47	Bi-dir	Not Reset Signal (From & To Evaluator-7T Board)
FPGACLK	77	Input	40MHz (modifiable) Generic Clock Input
Processor Interface Ports			
SDCLKIN	80	Input	System Clock/SDRAM Clock Out from processor
Addr0	108	Input	Address bus bit 0 (lsb)
Addr1	109	Input	Address bus bit 1
Addr2	110	Input	Address bus bit 2
Addr3	111	Input	Address bus bit 3
Addr4	112	Input	Address bus bit 4
Addr5	113	Input	Address bus bit 5
Addr6	114	Input	Address bus bit 6
Addr7	115	Input	Address bus bit 7
Data0	138	Bi-dir	Data bus bit 0 (lsb)
Data1	139	Bi-dir	Data bus bit 1
Data2	140	Bi-dir	Data bus bit 2
Data3	141	Bi-dir	Data bus bit 3
Data4	142	Bi-dir	Data bus bit 4
Data5	146	Bi-dir	Data bus bit 5
Data6	147	Bi-dir	Data bus bit 6
Data7	148	Bi-dir	Data bus bit 7
Data8	149	Bi-dir	Data bus bit 8
Data9	150	Bi-dir	Data bus bit 9
Data10	151	Bi-dir	Data bus bit 10
Data11	152	Bi-dir	Data bus bit 11
Data12	160	Bi-dir	Data bus bit 12
Data13	161	Bi-dir	Data bus bit 13
Data14	162	Bi-dir	Data bus bit 14
Data15	163	Bi-dir	Data bus bit 15
nEC0	37	Input	Not External I/O Chip Select 0
nOE	45	Input	Not Output Enable
nWBEO	58	Input	Not Write Byte Enable 0
nEWait	44	Output	Not External Wait Signal
XINTREQ0	17	Output	External Interrupt Request 0
EXTMREQ	101	Output	External Bus Master Request (Tied inactive)
CLKOE	46	Output	System Clock/SDRAM Clock Enable (Tied active)
Modem Interface Ports			
RxData	73	Input	Receive serial data input
TxData	69	Output	Transmit serial data output
nCTS	71	Input	Modem CLEAR TO SEND signal (active low).
nRTS	70	Output	Modem REQUEST TO SEND signal (active low).
nDSR	82	Input	Modem DATA SET READY signal (active low).
nRI	75	Input	Modem RING INDICATOR signal (active low).
nDCD	83	Input	Modem DATA CARRIER DETECT (active low).

Register Addressing

With the PPCI bridge generics set up as they are, bits 7:6 of the address bus are used to select which IP core is accessed (00 = StdUart, 01 = Watchdog), and bits 5:0 of the address bus are used to select which register in the IP core is accessed. With the processor interface to the FPGA set up by the modified Evaluator-7T eCos files, the IP core registers will be available at the following addresses (with cache disabled):

StdUart IP Core Registers

Address	StdUart Register
0x07A00000	RHR / THR / DivLo
0x07A00004	IER / DivHi
0x07A00008	ISR / FCR
0x07A0000C	LCR
0x07A00010	MCR
0x07A00014	LSR
0x07A00018	MSR
0x07A0001C	Scratchpad

Watchdog IP Core Registers

Address	StdUart Register
0x07A00100	TIMEOUT
0x07A00104	PULSELEN
0x07A00108	RSTTIMEOUT
0x07A0010C	RSTCOUNT

For full details of the individual registers, refer to the IP cores' datasheets.

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